REMARKS

The present amendment is in response to the latest Office Action, in which all pending claims are rejected. Applicants have thoroughly reviewed the outstanding Office Action including the Examiner's remarks and the reference cited therein. Applicants have further amended the claims by canceling claims 21 and 22 and adding these limitations to claim 1, which has been twice amended. Applicants most respectfully submit that all of the claims now present in the application are in full compliance with 35 USC 112 and are clearly patentable over the references of record.

The rejection of claims 21 and 22 under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention has been carefully considered but is most respectfully traversed.

Applicants most respectfully submit that the subject matter of the specification must be viewed in light of the level of skill of one of ordinary skill in the art to which the invention pertains. Initially, Applicants emphasize that both the specification and the drawings can be used to support the scope of the claims as these would be interpreted by one ordinary skill in the art. In this regard, Applicants most respectfully submit that one of ordinary skill, considering sequentially, by referring to the original Figs. 2A-2C, that it is clear that coating layer 22 covers all semiconductor structures 21 on substrate 20 and totally fills the gap(s) between neighboring semiconductor structures 21.

Similarly, by referring to the original FIGS. 2A-2C, it is clear that over coating layer 24 is located over all semiconductor structures 21 and then none of gap(s) is filled by the over coating layer 21. Therefore, Applicants most respectfully submit that one of ordinary skill in the art would reasonably interpret the specification, including the drawings, that Applicants had possession of the invention in both claims 21-22 which are supported by the original drawings. In other words, there is no new matter added in the previous amendment and it is most respectfully requested that this rejection be withdrawn. Reconsideration and withdrawal of the rejection under 35 U.S.C. 112(2) is respectfully requested.

Applicants have canceled claims 21 and 22 and have incorporated these claims into the corresponding independent claim 1, such that the scope of the amended independent claim is significantly different and unobvious over the combination of all cited prior arts. Hence, all corresponding dependent claims are automatically patentable for they only further limit the scope of the independent claim 1.

In response to Applicants' argument in the previous amendment that Donley is in contrast to his claimed invention, the Examiner considers that a prior art meets the claim if it is capable of performing the intended use.

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In response to Applicants' argument that Donley's process has additional steps, the Examiner considers that Donley discloses all of the steps required by Applicants' invention.

In response to Applicants' arguments that the Examiner's conclusion of obviousness is based upon improper hindsight, the Examiner considers that the variation of results effective process parameters, such as etching rate, is well known and an obvious step to one of ordinary skill in the art. Applicants respectfully traverse the Examiner's response to arguments.

Initially, Applicants emphasize that the arguments filed 4/11/02 is in response to the former office action that claims 1, 5, 7-8 and 10-11 are rejected under 35 U.S.C. 102(b) and depend claims 2-4, 6, 9 and 13-20 are rejected under 35 U.S.C. 103(a). Herein, the main difference between independent claim 1 and independent claim 13 is the step of CMP, which is not the main character(s) of the invention, and the independent claim 20 only is another vision of the independent claim 1. Thus, the argument filed 4/11/02 focused on traversing the rejection of independent claim 1 under 35 USC 102(b) and considered claims 2-20 are automatically patentable after independent claim being patentable for they are dependent claims or independent claims without new scope.

Therefore, while the rejection under 35 U.S.C. 102(b) being traversed but the rejection 35 U.S.C. 103(a) being more complicated than the former Office Action, it is reasonable that the arguments filed 4/11/02 are not persuasive.

However, in response to the Examiner's new reasons for rejection under 35 U.S.C. 103(a), Applicants also present new arguments, which comprises partial arguments filed 4/11/02, to traversed the Examiner's new reasons for rejecting. Please refer to the following arguments shown in the papers.

Sequentially, Applicants emphasize that claims 21-22 are incorporated into claim 1 now and then the scope of clams 1-12 is further limited. Therefore, it is reasonable that each rejection about claim 1 is automatically failed except it discloses or teaches the scope of claims 21-22.

Thirdly, in responses three Examiner's viewpoints shown in the current Response to Arguments, Applicants agree with the rules disclosed by the Examiner. However, Applicants disagree with the way that the Examiner uses the rules. For example, even the Examiner cites Jillie to support his viewpoints that the variation of result effective process parameters is a well know and obvious step to those of ordinary skill in the art, Applicants still disagree with the Examiner's viewpoint for both Jillie being strongly different than the claimed invention and Jillie itself claiming a specific order of etching power.

Therefore, if the Examiner's viewpoint being correct, Jillie should be unpatentable. Thus, while Jillie's specific etching power order being patentable, the specific order of etching rate of the claimed invention also could be patentable. In short, the patentability of the claimed invention should be decided by whether the specific order of etching rate is disclosed or taught, but should not be denied for the reason of the specific order being adjustable.

Finally, because new reasons and new cited prior art are present by the Examiner to rejected the claimed invention under 35 U.S.C. 103(a), Applicants present new arguments to traverse the rejection under 35 U.S.C. 103(a). Please refer to the following arguments shown in the paragraphs below "CLAIM REJECTIONS – 35 U.S.C. SECTION 103(a)."

CLAIM REJECTIONS – 35 U.S.C. SECTION 103(a)

Claims 1, 3-11 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Donley (U.S. 4,299,862) in view of Jillie, Jr. et al. (Hereinafter Jillie) (U.S. 4,808,259). And Claims 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Donley in view of Jillie and Obeng (U.S. 5,836,805).

By referring to col. 2 lines 64-67, col. 3 lines 25-26, col. 4 lines 41-44 and 61-63, col. 5 lines 64-67, Figure 3 and Figure 13 of Donley, the Examiner considers that Donley does not discloses the etching rate of the overcoating layer is higher than the etching rate of the coating layer not does not discloses the preferred angles. Moreover, the Examiner also considers that Donley is silent about planarizing its silicon dioxide dielectric layer, and the Examiner also considers that Donley's Figures 9-10 shows the scope of claims 21-22.

However, by referring to col. 2 lines 30-38 and col. 4 lines 38-44 of Jillie, the Examiner considers that Jillie discloses a semiconductor manufacturing method and further discloses that the variation of process parameters during semiconductor manufacturing is obvious to one skilled in the art.

However, by referring to col. 1 lines 11-31 of Obeng, the Examiner considers that Obeng discloses the step of planarizing the dielectric layer by CMP (chemical mechanic polishing).

Therefore, it is the Examiner's position that it would have been obvious to one of ordinary skill in the art at the time of the invention to vary etching rate, angle and any other parameters, in view of Jillie's disclosure that this is an obvious step, common during semiconductor manufacturing.

Therefore, it is the Examiner's position that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Donley by planarizing the dielectric layer by CMP, as per Obeng, since Obeng himself provides the motivation to do so: increased reliability or devices, which is highly desirable.

Furthermore, it also is the Examiner's position that etching rate and viscosity are result effective variables, and its variation would have been obvious to one of ordinary

skill in the art at the time of the invention, with the purpose of establishing the optimum process mode.

Applicants respectfully traverse this rejection.

Applicants briefly summarize their reasons for traversing as the following:

(a) Donley does not disclose or teach the scope of claims 21-22.

(b) Claims 21-22 are incorporated into independent claim 1.

(c) Jillie's invention is related to a specific order of etching power. Thus, Jillie only discloses values of process parameters, which are not the key of his invention, are adjustable.

(d) The claimed specific order of etching rate is not disclosed or taught by any cited prior art.

(e) None of the cited prior arts has the motivation of have the claimed specific order of etching rate.

(f) How to planarize is not the main character of the claimed invention. Thus, the patentability of the claimed invention is independent on Obeng.

Regarding to (a), Applicants emphasize the following comparison between the claimed invention and Donley:

The claimed invention	Donley
semiconductor structure	electrode 18a
coating layer	silicon dioxide layer 14b
over coating layer	silicon nitride layer 24
gaps between semiconductor structure	only one electrode without any gap

Therefore, for example, by considering the portion over region 20 and regions 22, it is clear that the total thickness of silicon dioxide layer 14b and silicon nitride layer 24 is smaller than the thickness of electrode 18a. Please refer to FIG. 7 of Donley. Otherwise, Donley should at least show an uniform silicon dioxide layer 14 over substrate 10 in FIG. 6, or at least shown an uniform combination of silicon dioxide layer 14b and silicon nitride layer 24 over substrate 10 in FIG. 7, or should not show a L-type shape of both silicon dioxide layer 14b and silicon nitride layer 24.

In short, Applicants reasonably emphasize that the Examiner misunderstands Donley. In fact, Donley never discloses or teaches the scope of claims 21-22.

Regarding to (b), because claims 21-22 is not disclosed by any cited prior art, the combination of claim 1 and claims 21-22 is automatically patentable. Moreover, all dependent claims of independent claim 1 also are automatically patentable for they only further limiting the scope of the independent claim 1.

In other words, claims 1-12 are patentable now, no matter whether the relation of etching rates between the coating layer and the over coating layer is patentable.

Regarding to (c), Applicants initially emphasize the Examiner agrees Donley never discloses or teaches that the etching rate of the overcoating layer is higher than the etching rate of the coating layer. In other words, if the Examiner's viewpoint of Jillie being traversed and the Examiner's viewpoint about "the variation of result effective process parameters" being traversed, all pending claims are automatically patentable for one main character being not disclosed or taught by any cited prior art.

By carefully analyzing Jillie, Applicants find that Jillie utilizes a multiple step power reduction recipe. In other words, Jillie limits the power of each following etch process must be lower than the power of the former etch process. Please at least refer to col. 1 lines 53-61, col. 2 lines 4-17, col. 2 lines 27-38, col. 2 lines 59-68, col.3 line 64 to col. 4 lines 12, col. 4 lines 38-56.

Clearly, Jillie claimed a method of sequentially etching a thin film with several power level, where each power level used by one etch process is lower than the power level used by the former etch process. For examples, Jillie's first embodiment uses 275 watts and 150 watts in sequence, and Jillie's second embodiment uses 275 watts, 150 watts, 100 watts and 75 watts in sequence. Clearly, Jillie does not limit the practical power used to etch. In contrast, Jillie really limits a specific order of etching power: for a series etching process, the power is reduced in sequence.

Additional, Jillie never discloses or teaches anything about the different etching rates between neighboring layers. In other words, Jillie is nothing about the main character and the issue of the claimed invention. This can be proven by using "etch" and "rate" as the key-words to thoroughly search Jillie.

Therefore, although Jillie really discloses the idea of "the variation of process parameters during semiconductor manufacturing is obvious to one skilled in the art", Jillie still limits and claims a specific order of etching power. In other words, Jillie not only means that the values of parameters are adjustable for one skilled in the art, Jillie further means that the specific order of parameter(s) could be patentable.

Therefore, while Jillie's specific order of etching power being an allowed patent, the order or etching rate present by the claimed invention also could be patentable (the claimed invention never limits the practical etching rate of each rates). At least, the patentability of the claimed invention should not be rejected by only referring to Jillie and considering Jillie disclosing that the variation process parameters are obvious.

Accordingly, Applicants reasonably emphasize that the difference(s) between the claimed invention and Donley is (are) not disclosed or taught by Jillie. Thus, none of the pending claims is unpatentable over Donley in view of Jillie.

Regarding to (d), Applicants agree with the Examiner's viewpoint of Obeng, and essentially agrees the Examiner's viewpoint of the differences between the claimed invention and Donley. Moreover, as discussed above, Jillie is nothing about the etching rates between neighboring layers.

Therefore, Applicants reasonably emphasize that "the etching rate of the over coating layer is larger than the etching rate of the coating layer" never is disclosed by Donley, Jillie and Obeng.

Regarding to (e), because Jillie never discloses "any order of process parameters" is obvious to one skilled in the art, the Examiner's position that "it would have been obvious to one of ordinary skill in the art at the time of the invention to vary etching rates, angles and any other parameters, in view of Jillie's disclosure that this is an obvious step, common during semiconductor manufacturing" is automatically failed. Note that Jillie itself claims a specific order of etch power of sequentially etching process. Hence, Jillie never discloses "a specific order of some process parameters are obvious", and then the combination of Donley and Jillie still is different than the fact that "a specific order of etching rates of neighboring layers" is obvious.

Further, the claimed invention is related to the issue of how to form a contact hole which is easily to be filled, but Donley is related to the issue of how to prevent

improper lateral etch. Indisputably, Donley and the claimed invention corresponds to two significantly different technology field. Hence, it is not obvious to refer Donley for archiving the issue of the claimed invention.

Besides, by at least referring to col. 6 lines 7-45, Donley achieves its issue by let the etching rate of silicon nitride layer 24 be higher than the etching rate of silicon oxide layer 14b, such that the undesired lateral etching during the formation of the contact hole is prevented by the existence of silicon nitride layer 24. Therefore, because the location of Donley's silicon oxide layer 14b corresponds to the location of the coating layer of the claimed invention and the location of Donley's silicon nitride layer 24 corresponds to the location of coating layer of the claimed invention, it is not direct and natural to acquire the claimed invention by amending the prior art and only referring to Donley.

In short, Applicants reasonably emphasize that Donley does not have the motivation of have the claimed specific order of etching rate.

Further, both Jillie and Obeng are nothing about the claimed specific order of etching rate, also are nothing about the contact window in dielectric layer, such as coating layer. Thus, Applicants reasonably emphasize that both Jillie and Obeng do not have the motivation of have the claimed specific order of etching rate.

As a short summary, regarding to (a) and (b), Applicants reasonably believe that claims 1-12 are patentable now, because claims 1-12 comprise the scopes of "the semiconductor structure is thicker than the coating layer and the over coating layer" and "the gap between neighboring semiconductor structure is not filled by the over coating layer". Moreover, regarding to (c), (d) and (e), Applicants reasonably believe claims 1-20 and claims 13-20 also are patentable, because claims 1-20 comprise the scope of "the etching rate of over coating layer is higher than the etching rate of coating layer". Herein, as the Examiner considered, "etching rate" and "viscosity" are result effective variables.

Reconsideration and withdrawal of the rejection under 35 U.S.C. 103(a) is respectfully requested.

In view of the above comments and further amendments to the specification and claims, favorable reconsideration and allowance of all of the claims now present in the application are most respectfully requested.

Respectfully submitted,

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Marked-Up Version of Changes Made

IN THE CLAIMS:

Please delete claims 21 and 22 without prejudice or disclaimer.

Please replace claim 1 with the following amended claim 1.

1(Twice Amended). A method for forming a contact window, said method comprise:

forming a plurality of semiconductor structures on a wafer, wherein a plurality of gaps are located between neighboring semiconductor structures;

forming a coating layer over the surface of said wafer, where the thickness of said coating layer is not less than the heights of said semiconductor structures; wherein said semiconductor structures are covered by said coating layer and said gaps are totally filled by said coating layer;

forming an over coating layer over said coating layer, wherein the etching rate of said over coating layer is higher than the etching rate of said coating layer, wherein said gaps are not filled by said over coating layer; and

forming said contact window in both said over coating layer and said coating layer. wherein upper part of said contact window is outwardly widened.